Micromega Corporation

Application Note 43

Speed and Power Considerations for uM-FPU V3

Introduction

This application note discusses speed and power considerations when using the uM-FPU V3 floating point coprocessor. Processing speed and power consumption are directly related. The higher the processing speed, the higher the power consumption, but the uM-FPU V3 chip has two power saving modes that can be used to reduce power consumption. Information in this application note can help you design for both high speed and low overall power consumption.

Processing Speed

The speed of the FPU is determined by the clock frequency, which in turn is limited by the operating voltage. The maximum clock frequency is as follows:

Operating Voltage	Maximum Clock Frequency
4.5V to 5.5V	30MHz
3.0V to 5.5	15 MHz
2.5V to 5.5V	7.5 MHz

Power Consumption

The power consumption of the FPU depends on the operating voltage, clock speed, and the proportion of time spent in Full speed, Idle, or Sleep modes. Figure 1 (at the end of the document) shows the relationship between the various factors. Power consumption is lower for lower operating voltages, but the maximum clock speed must also be reduced at lower operating voltages. For a given operating voltage, the current draw is proportional to the clock speed. If the clock speed is cut in half, the current draw is reduced by approximately half, but a given calculation will take twice as long. Current draw is also reduced by approximately half by switching from Full speed mode to Idle mode.

Most applications don't perform floating point calculations continuously. They sample values periodically, then perform the necessary calculations. As a result, there are often large periods of idle time. By default, the FPU will automatically switch to Idle mode when not actively performing a calculation.

The lowest power consumption is achieved through the use of Sleep mode. With an operating voltage of 5V, the FPU uses only 10-20 microamps when in Sleep mode. For applications that only perform periodic calculations, the FPU can be put into Sleep mode between calculations. As the ratio of Full speed calculations to Sleep mode gets smaller, the average power consumption will approach the 10-20 microamp minimum.

Idle Mode Power Saving

Idle mode power saving is enabled by default on the uM-FPU V3.1 chip. When the last instruction instruction finishes execution and the instruction buffer is empty, the uM-FPU V3 chip will enter Idle mode and the supply current will drop to approximately half the current used at full speed (see Figure 1). The chip will return to full speed when the next instruction is received. The Idle mode power saving can be disabled by clearing bit 4 of mode parameter byte 0. The parameter bytes can be set or cleared using the *uM-FPU V3 IDE* software and the *Set Parameters...* menu command.

Sleep Mode Power Saving

Sleep mode power saving can be used to greatly reduce the power requirements of the uM-FPU V3 chip. In sleep mode the supply current for the chip drops to approximately 10 to 20 microamps. To enable Sleep mode, bit 3 of mode parameter byte 0 must be set. The CS pin is used to wake up the FPU. Since the CS pin is used for Sleep mode, the interface mode (bits 1:0 of mode parameter byte 0) must be set to either 01 for I^2C or 1x for SPI. The parameter bytes can be set or cleared using the *uM-FPU V3 IDE* software and the *Set Parameters...* menu command.

Sleep mode is entered under the following conditions:

- the last instruction finishes execution
- the instruction buffer is empty
- Interface mode (bits 1:0 of mode parameter byte 0) is set to 01 for I^2C, or 1x for SPI
- Sleep mode power saving (bit 3 of mode parameter byte 0) is set to 1
- the debug monitor is disabled
- the CS pin is high

The uM-FPU V3.1 chip wakes up under the following conditions:

- the CS pin goes low

Note: After the CS pin goes low, a 500 microsecond delay is recommended before any instruction bytes are sent to allow the FPU to wake up.

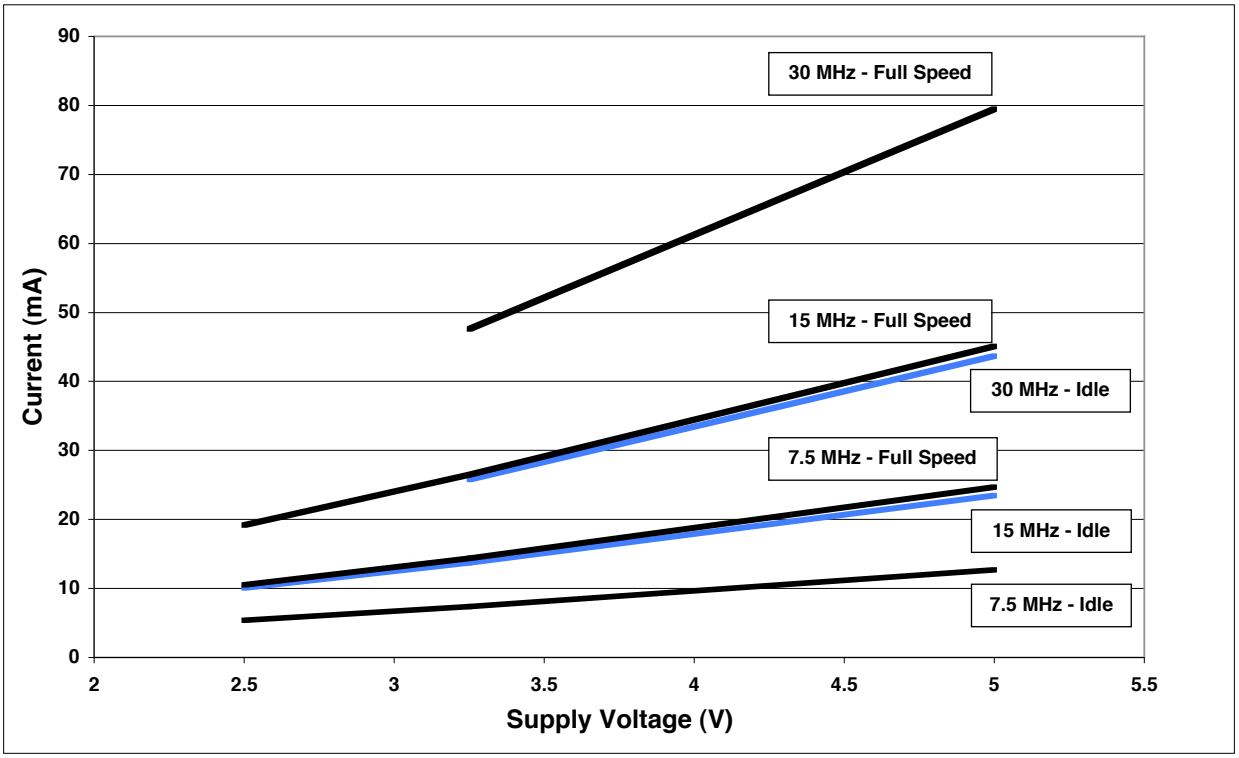
Current vs Supply Voltage

Current measurements were taken at 0.25V intervals for the six different operating conditions shown in Table 1. The results are linear, so only the endpoints are shown in Table 1. The linear relationship between current and supply voltage is shown in Figure 1.

Table 1 - Current Measurements

Supply Voltage (V)	30MHz Full Speed (mA)	30 MHz Idle (mA)	15 MHz Full Speed (mA)	15 MHz Idle (mA)	7.5 MHz Full Speed (mA)	7.5 MHz Idle (mA)
5	79.5	43.7	45.1	23.5	24.7	12.7
3.25	47.6	25.8	26.5	13.7	14.4	7.4
2.5	-	-	19.2	10.1	10.5	5.4

Figure 1 - Current vs Supply Voltage



Note: For a clock frequency of 30MHz, operating voltage should be 4.5V to 5.5V
For a clock frequency of 15 MHz, operating voltage should be 3.0V to 5.5V
For a clock frequency of 7.5 MHz, operating voltage should be 2.5V to 5.5V

Further Information

See the Micromega website (http://www.micromegacorp.com) for additional information regarding the uM-FPU V3.1 floating point coprocessor, including:

uM-FPU V3.1 Datasheet
uM-FPU V3.1 Instruction Set
Using the uM-FPU V3 Integrated Development Environment (IDE)